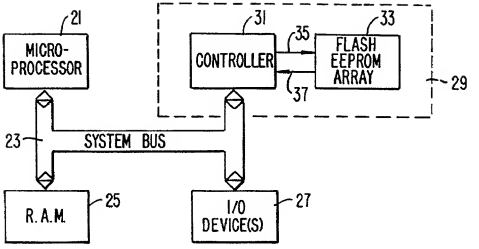

21
MICRO-
PROCESSOR
31
CONTROLLER
35
33
FLASH
EEPROM
ARRAY
37
29
23
SYSTEM BUS
R.A.M.
25
I/O
DEVICE(S)
27

FIG._1A

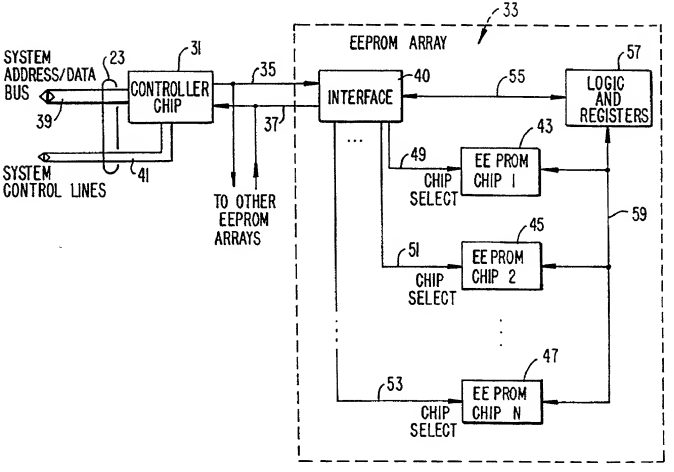

33
EEPROM ARRAY
SYSTEM
ADDRESS/DATA
BUS
23
39
31
CONTROLLER
CHIP
35
37
41
SYSTEM
CONTROL LINES
TO OTHER
EEPROM
ARRAYS
INTERFACE
40
55
57
LOGIC
AND
REGISTERS
49
CHIP
SELECT
43
EE PROM
CHIP 1
59
51
CHIP
SELECT
45
EE PROM
CHIP 2
53
CHIP
SELECT
47
EE PROM
CHIP N

FIG._1B

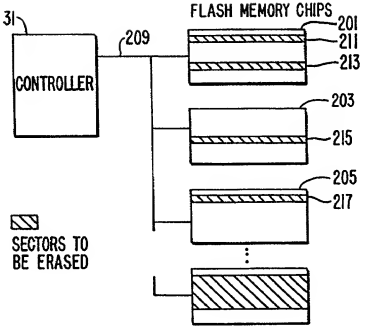


FIG._2

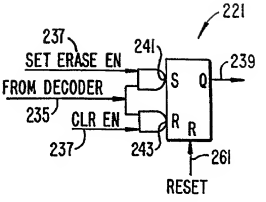


FIG._3B

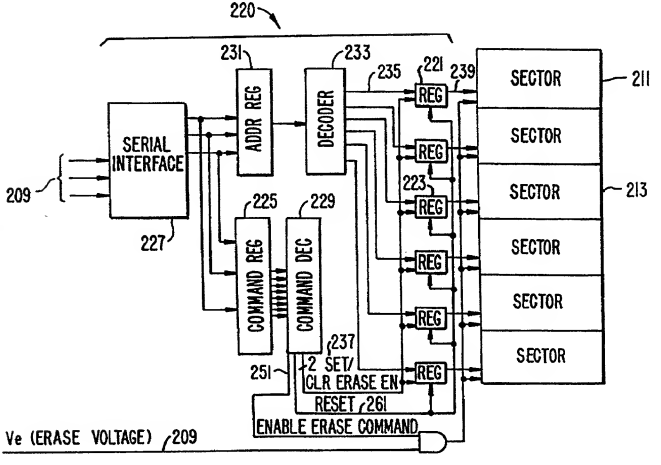


FIG._3A

08879886.050301

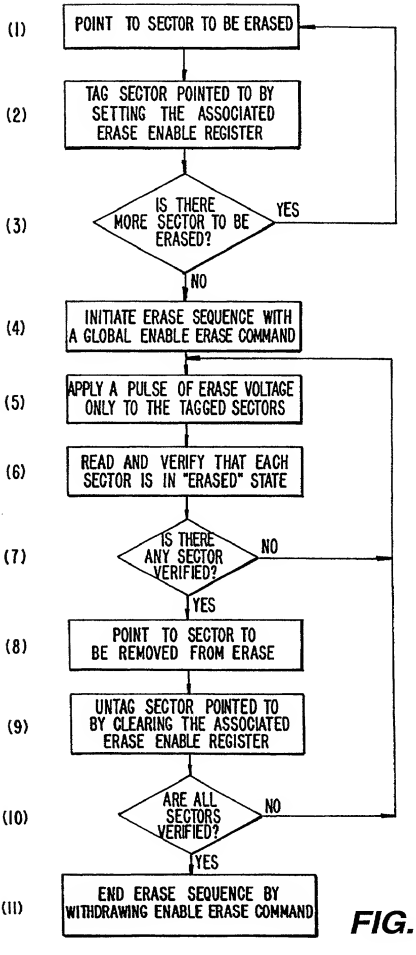


FIG._4

0686785.052001

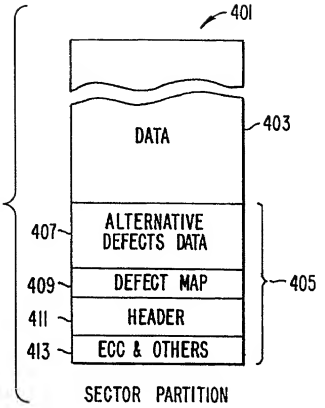


FIG._5

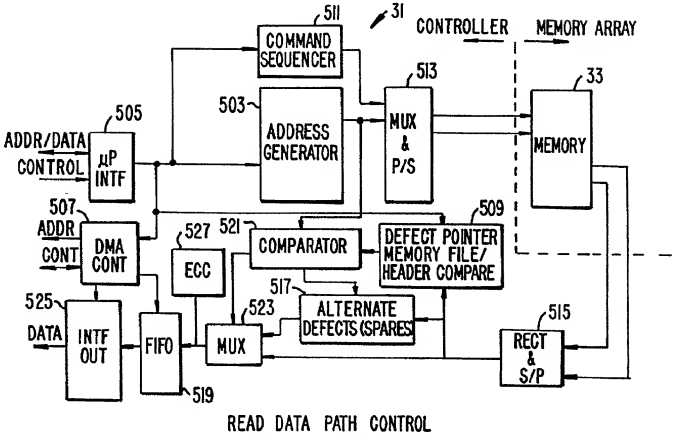


FIG._6

0068783 05300

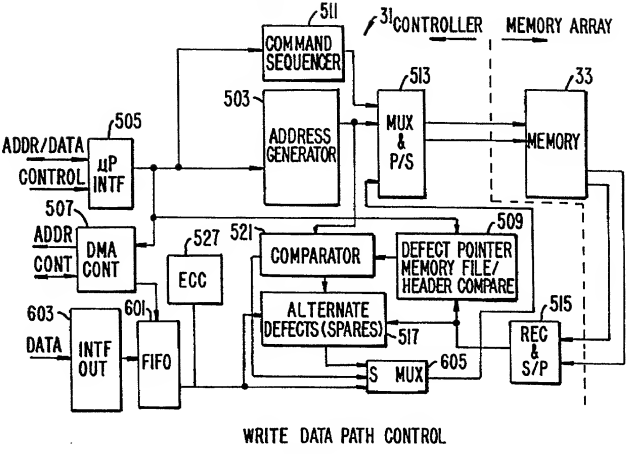


FIG._7

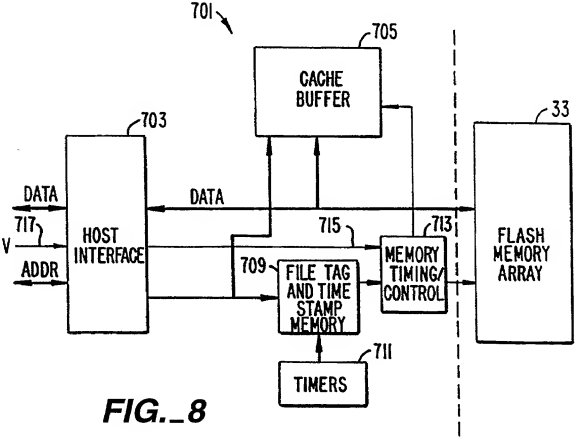


FIG._8

0056836 "05200.01

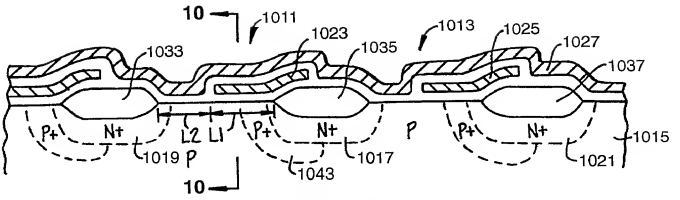


FIG._9

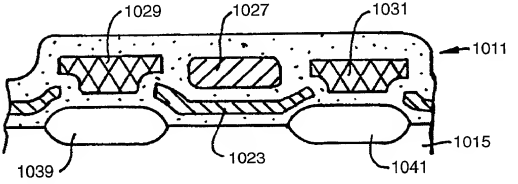


FIG._10

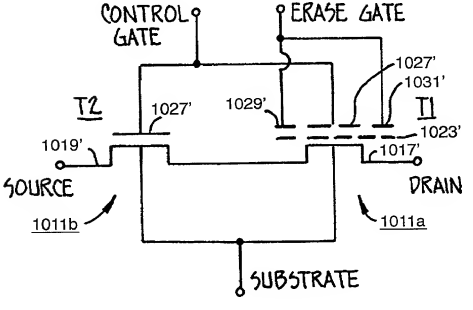


FIG._11

09857836.050301

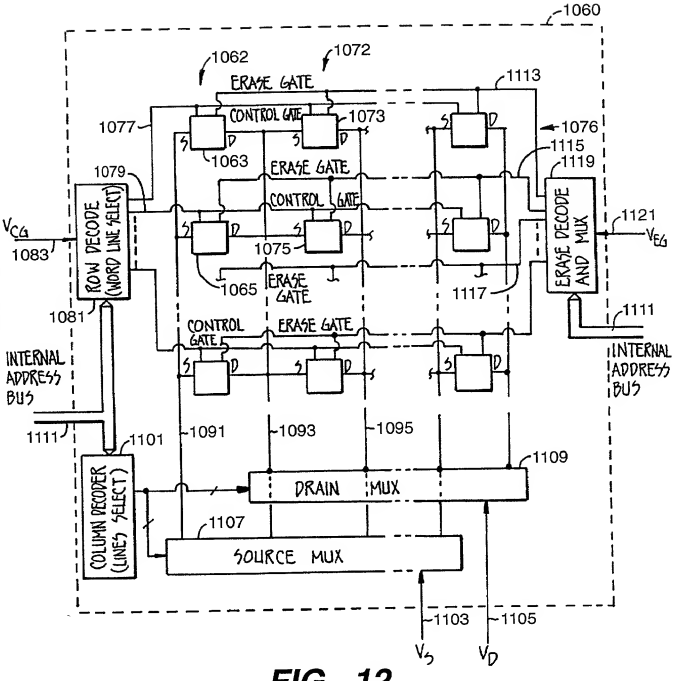

1060
1062
1072
ERASE GATE
1113
CONTROL GATE
1073
1077
1076
1063
1115
1119
ERASE GATE
1079
CONTROL GATE
ROW DECODE (WORD LINE SELECT)
ERASE DECODE AND MUX
1121
V_{CG}
1083
1075
V_{EG}
1065
ERASE GATE
1117
1081
1111
CONTROL GATE
ERASE GATE
INTERNAL ADDRESS BUS
INTERNAL ADDRESS BUS
1111
1101
1091
1093
1095
1109
COLUMN DECODER (LINES SELECT)
DRAIN MUX
1107
SOURCE MUX
1103
1105
V_S
V_D

FIG._12

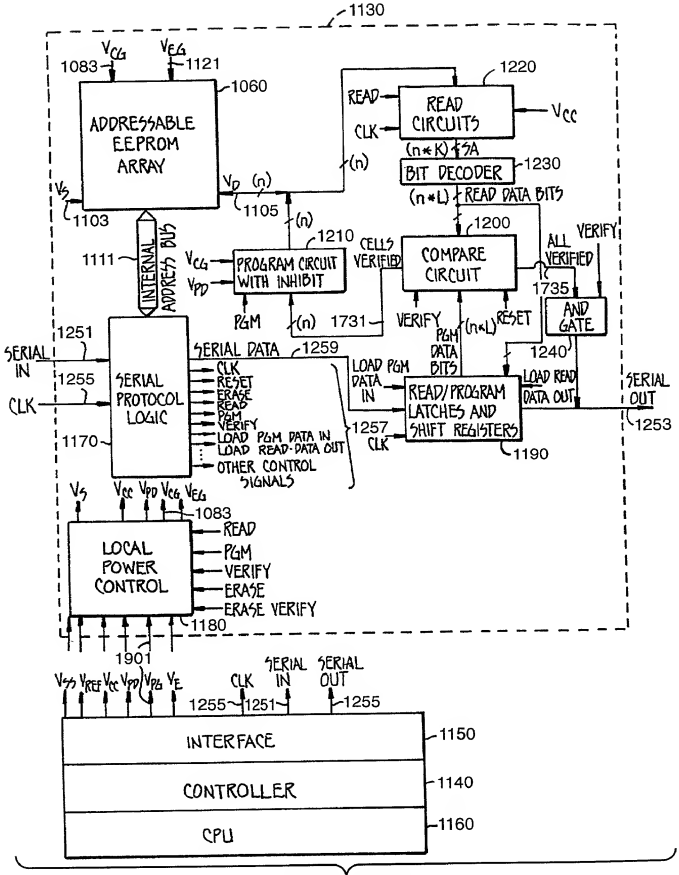

1130
ADDRESSABLE E.E.PROM ARRAY
1060
1083
1121
1103
1105
INTERNAL ADDRESS BUS
1111
1210
PROGRAM CIRCUIT WITH INHIBIT
READ
CLK
READ CIRCUITS
1220
BIT DECODER
1230
READ DATA BITS
1200
COMPARE CIRCUIT
CELLS VERIFIED
ALL VERIFIED
VERIFY
1735
AND GATE
RESET
1240
1731
PGM DATA BITS
LOAD PGM DATA IN
LOAD READ DATA OUT
READ/PROGRAM LATCHES AND SHIFT REGISTERS
1190
1257
1251
SERIAL IN
1255
CLK
SERIAL PROTOCOL LOGIC
1170
SERIAL DATA
1259
RESET
ERASE
READ
PGM
VERIFY
LOAD PGM DATA IN
LOAD READ DATA OUT
OTHER CONTROL SIGNALS
SERIAL OUT
1253
LOCAL POWER CONTROL
1180
ERASE VERIFY
1901
INTERFACE
1150
CONTROLLER
1140
CPU
1160

FIG._13

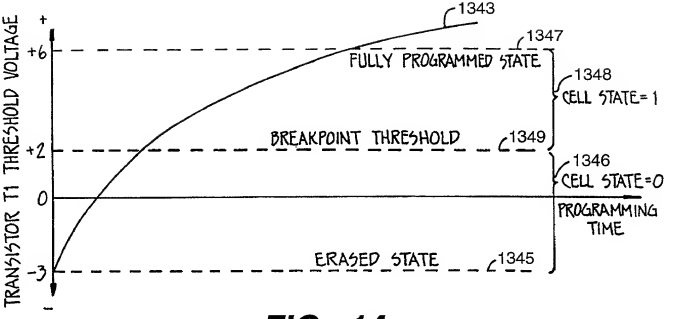


FIG._14

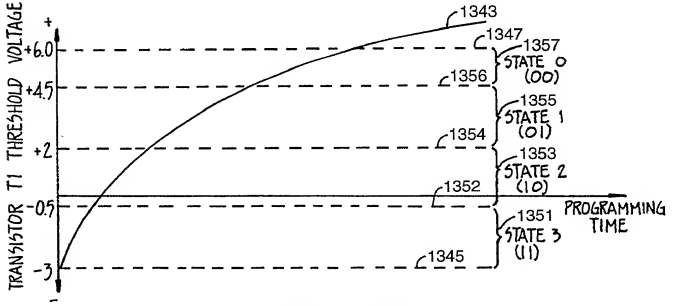


FIG._15A

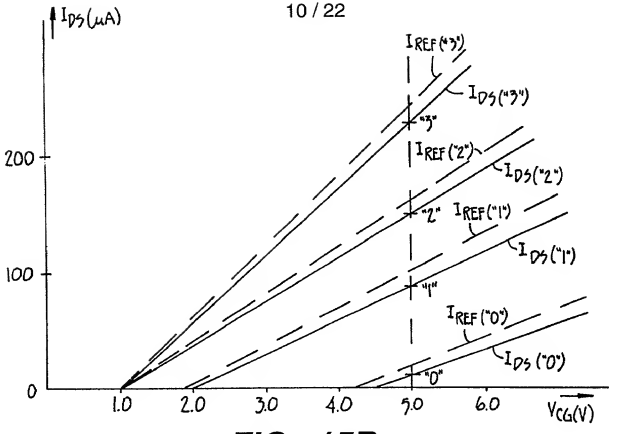


FIG._15B

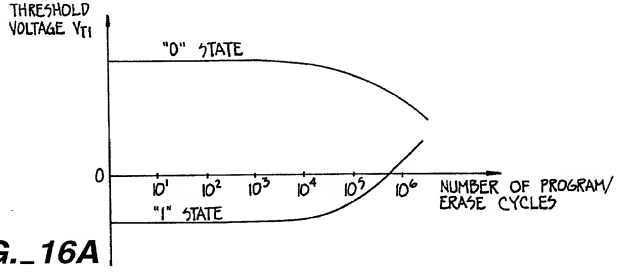


FIG._16A

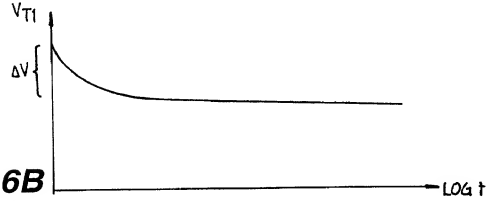


FIG._16B

10025/0 SE87980D

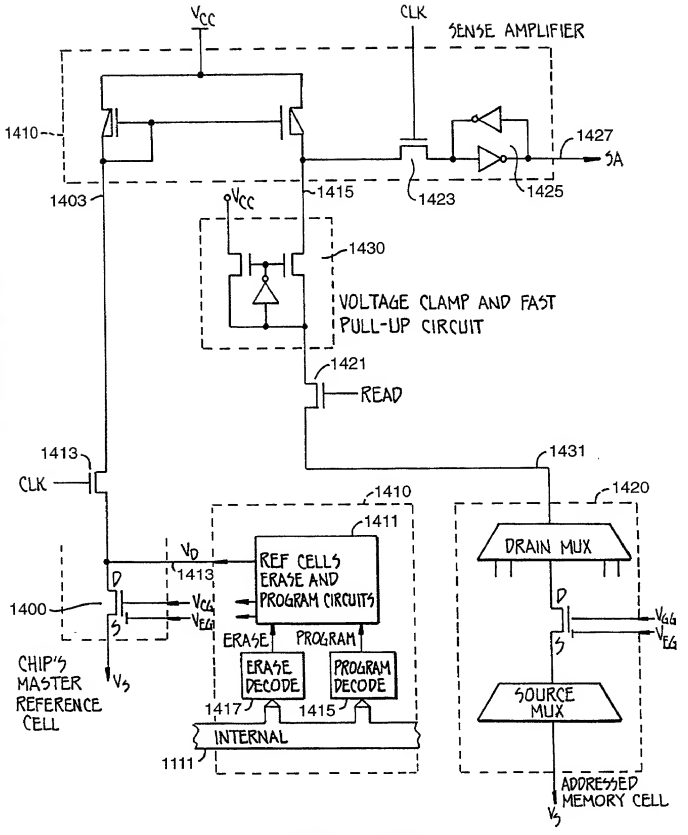


FIG._17A

09867836.053001

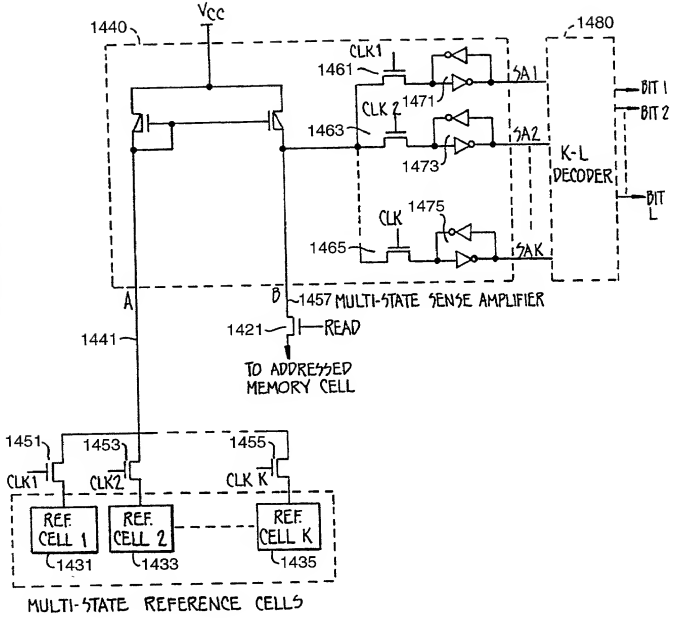


FIG._17B

09867836 - 050501

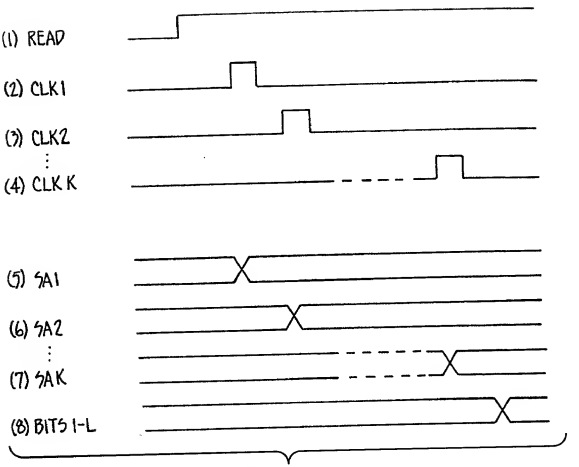


FIG._17C

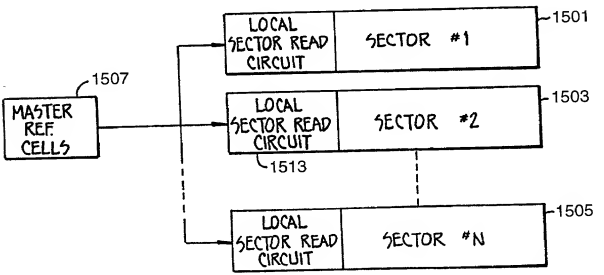


FIG._18

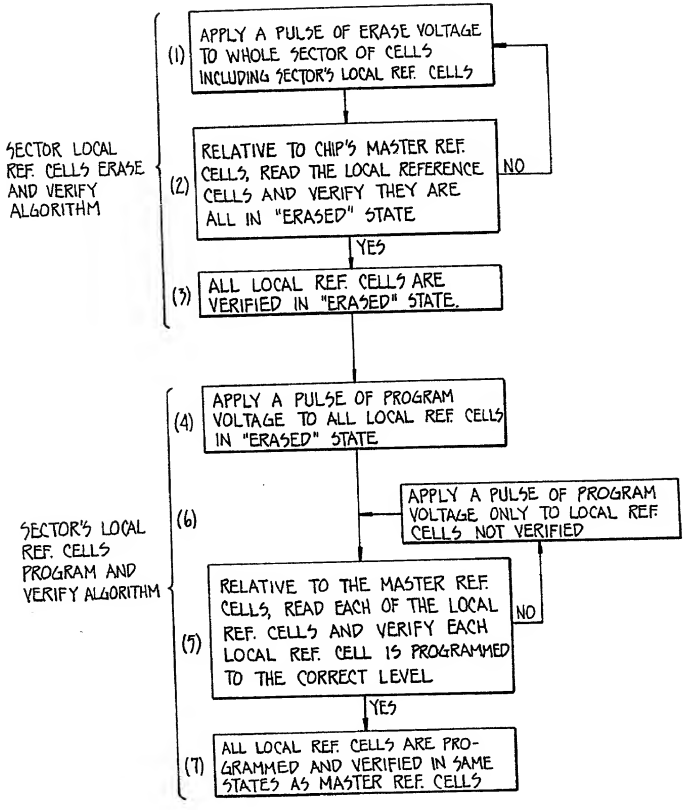


FIG._19

0988273350.055001

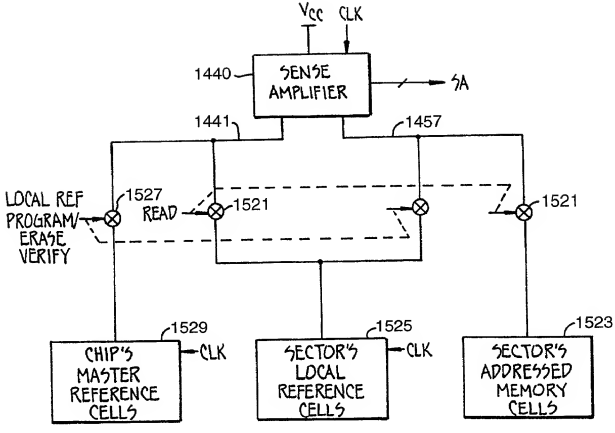


FIG._20A

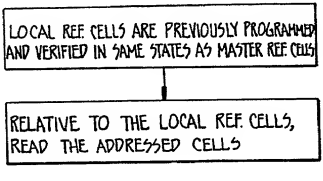
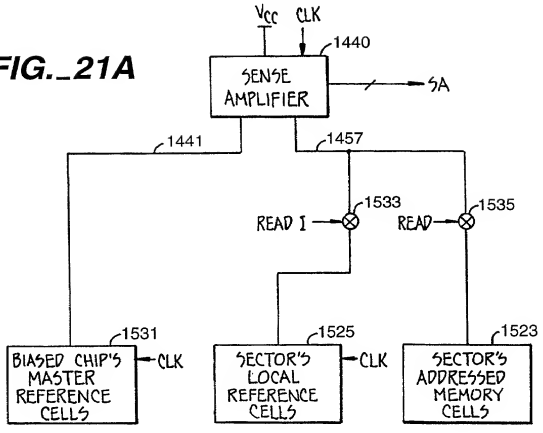


FIG._20B

FIG._21A



09867236-052801

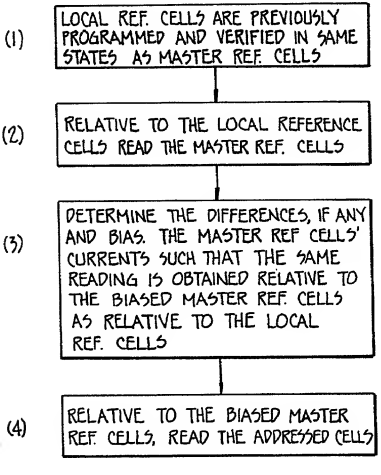


FIG._21D

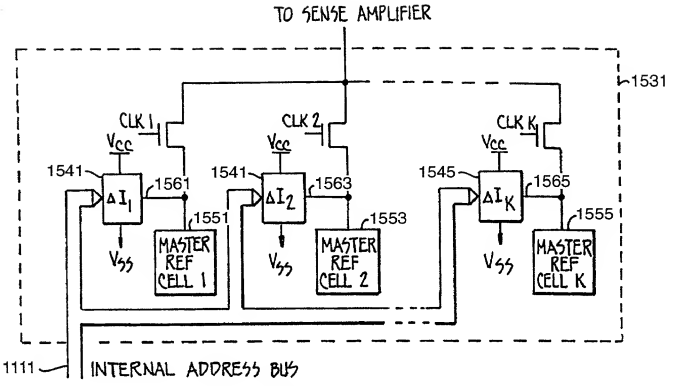


FIG._21B

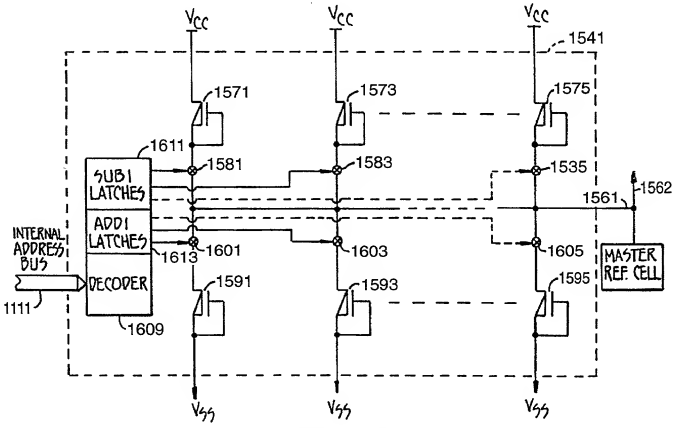
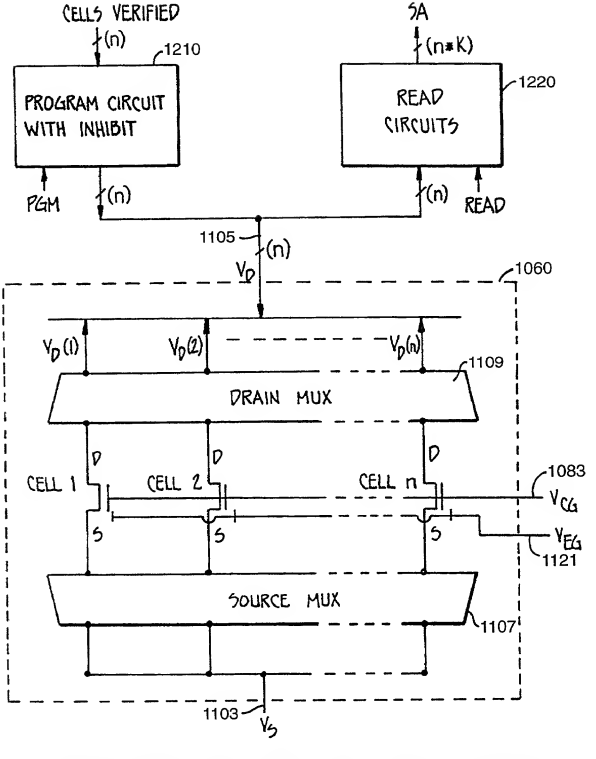
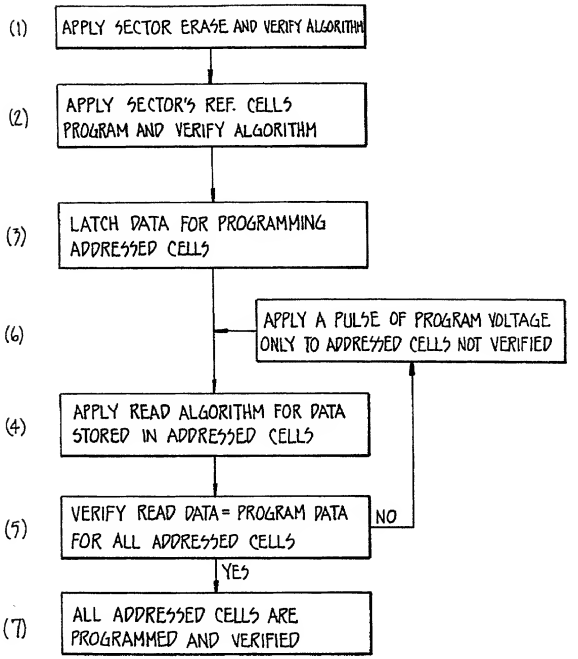


FIG._21C



READ/PROGRAM DATA PATHS FOR n CELLS IN PARALLEL

FIG._22



PROGRAM ALGORITHM

FIG._23

09867835 - 053001

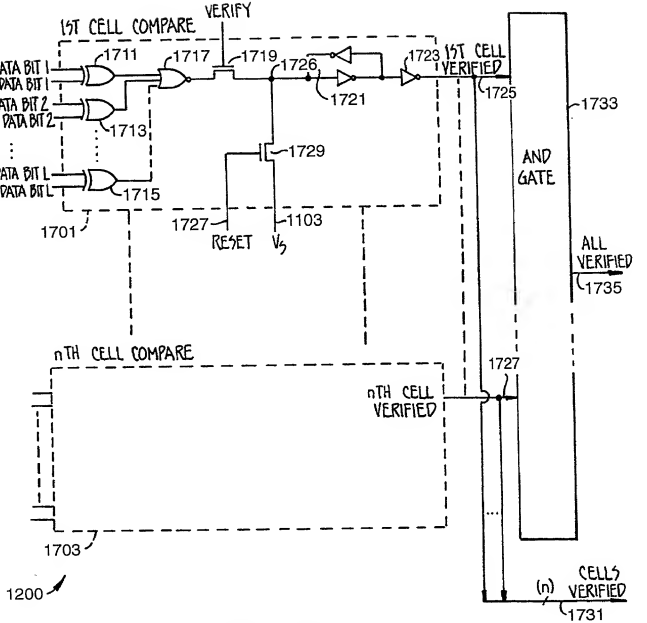


FIG._24

09887986 - 052601

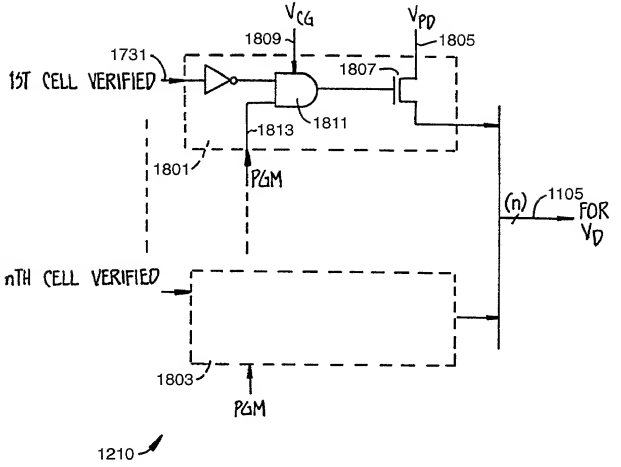

V_{CG}
V_{PD}
1809
1805
1731
1807
1ST CELL VERIFIED
1813
1811
1801
PGM
(n)
1105
FOR V_D
nTH CELL VERIFIED
1803
PGM
1210

FIG._25

	SELECTED CONTROL GATE V_{CG}	DRAIN V_D	SOURCE V_S	ERASE GATE V_{EG}
READ	V_{PG}	V_{REF}	V_{SS}	V_E
PROGRAM	V_{PG}	V_{PP}	V_{SS}	V_E
PROGRAM VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E

TABLE 1

FIG._26

(TYPICAL VALUES)	READ	PROGRAM	PROGRAM VERIFY	ERASE	ERASE VERIFY
V_{PG}	V_{CC}	12V	$V_{CC}+\delta V$	V_{CC}	$V_{CC}-\delta V$
V_{CC}	5V	5V	5V	5V	5V
V_{PP}	V_{SS}	8V	8V	V_{SS}	V_{SS}
V_E	V_{SS}	V_{SS}	V_{SS}	20V	V_{SS}
UNSELECTED CONTROL GATE	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
UNSELECTED BIT LINE	V_{REF}	V_{REF}	V_{REF}	V_{REF}	V_{REF}

V_{SS}=0V, V_{REF}=1.5V, δV=0.5V - 1V

TABLE 2

FIG._27

T00350 "SE879860